Ramp and Sinusoidal Histogram Methodologies for ADC Evaluation


School of Electrical and Electronic Engineering
Universiti Sains Malaysia, Engineering Campus
14300 Nibong Tebal, Seberang Perai Selatan, Pulau Pinang, Malaysia
Tel: +604-5995762, Fax: +604-5941023 (e-mail: aeizaa@usm.my)

Abstract: ADC production testing has become more challenging due to more stringent test procedure for new generation of ADC. The trend for silicon cost is going down while the cost of test is going up. Therefore, to reduce the cost of test and preserve the test accuracy is essential for high volume testing in production. This research objective is to develop test solutions for 28nm 10 bit ADC using histogram methodologies. The outcome from this research has clearly shows that the test program that has been developed is able to segregate the good and bad devices. 98.18% of the devices are able to pass the ADC testing while remaining 1.82% fail the ADC test. It was found that Ramp Histogram and Sinusoidal Histogram method has achieved this research objective as both methodologies shows similar result based on comparison that has been made. It was known that accurate ADC testing requires large sample size. This research found that multi-site testing was able to compensate the drawback in histogram methodologies. The result shows that multi-site testing is 63.72% more efficient in term of ADC testing time.

Keywords: Analog-to-Digital Converter(ADC), Offset Error, Gain Error.

1. INTRODUCTION

At present, most part of the signal processing in areas like instrumentation, telecommunications, and control is carried out at the digital domain. Therefore, ADC plays an important role to convert analog signal to digital signal. The presence of the ADC macro cells embedded in complex system on chip requires correct evaluation and testing using production tester as known as Automatic Test Equipment (ATE).

As the new generations of ADC provide increase in resolution and speed, the test requirements become more stringent and resulting in more expensive test procedures. The test cost frequently reaches half price of the device itself and this would increase the cost of the device in the end user market and forcing electronic manufacturer to offer competitive price. Test cost control is becoming important in the semiconductor industry because testing cost is increasing while the cost of silicon is decreasing. ADC is a key component of mixed-signal SOCs, so their testing is important. For high-resolution, slow sampling rate ADCs (such as SAR ADCs embedded in micro-controller chips), their DC linearity testing is very important but very time consuming, and hence costly (Uemori et al., 2010). Fig. 1 shows the trend for silicon cost going down while the test cost is going up. The cost for silicon is decreasing due to the cost per transistor is decreasing.

Test accuracy is essential in high volume production testing because accurate test methodology will prevent over reject in testing.

Fig. 1. Silicon Cost and Production Test Cost Trends (Uemori et al., 2010)

This work is focusing on ADC test methodology. In ADC testing using Automatic Test Equipment (ATE), analog input stimulus is generated by an arbitrary waveform generator (AWG) which employs a Digital to Analog Converter (DAC) and output code for each analog voltage conversion is measured using digital capture. ATE test system operation requires the test hardware to be used as interface card in between DUT and test system.
The most typical ADC output signal processing method is using Histogram analysis. Basically, there are two types of Histogram which is Ramp Histogram and Sinusoidal Histogram. Ramp Histogram method appears a flat line profile for linearity calculations. In Sinusoidal Histogram method, a very low distortion wave is required. However, since ADC generate non-flat histogram distribution for Sine wave; post processing of the Sinusoidal Histogram for linearity calculation becomes much more complex than Ramp Histogram (Okawara, 2009). The sine wave based method is called “dynamic linearity” because high frequency sine waves are easier to generate and the method can be used to evaluate the linearity of the ADC during dynamic input conditions. Sometimes the term “DC linearity” is used to denote that the “linearity” is measured at a very low conversion rate, using a DC-like, slowly varying input (Kuyel, 1999).

When testing the ADC, there are two types of ADC data to determine the performance of ADC which is static and dynamic performance. Static performance such as Differential non-Linearity (DNL), Integral non-Linearity (INL), Offset Error (OE) and Gain Error (GE) are the typical measurement of ADC during high volume production testing. Dynamic performance of ADC involve the measurement of the parameter induced by the noise level such as Signal to Noise and Distortion Ratio (SNDR), Total Harmonics Distortion (THD) and Spurious Free Dynamic Range (SFDR). Usually, dynamic performance of ADC is measured to characterize the noise level of the DUT (Chauhan et al., 2013). The noise could be generated from a few sources such as test equipment clock jitter, harmonics from test equipment, DUT’s input circuitry, DUT’s aperture jitter and DUT’s nonlinear distortion (Xu, 1999). In this research the focus is only on the static parameter of ADC because the study of dynamic parameter is more suitable for high resolution ADC.

In practice, both static and dynamic information on the ADC behaviour is usually needed, as well as figures showing its performance both in the time and frequency domains. It is widely recognized that, among other parameters, ADC Integral non-Linearity (INL) and Differential non-Linearity (DNL) represent quantities of paramount importance for the description of the tested device quality under both static and dynamic conditions.

To measure the ADC linearity parameters, the histogram test methodology is applied. This methodology is based on the use of a signal source exciting the ADC under test and the evaluation of the histogram analysis of the device output codes. Accordingly, the prior knowledge about the amplitude distribution of the converter input signal is employed (Azais et al., 2004). The linearity parameters are finally estimated by processing the ADC output code histogram. The most frequently used device input stimulus is the sinusoidal and ramp, even though Gaussian noise has been recently proposed as an alternative approach (Carbone et al., 2002).

The aim of this studies is to develop test solution for Analog to Digital Converter (ADC) in high volume production testing using histogram methodologies. This studies will help Test Engineer to be better understanding the concept behind ADC testing and aware of the factor that could induce the test performance of ADC in DSP based testing. Outcome from this research would help to improve ADC test accuracy and yield as well as production test time (Alegria et al, 2004). Organization could benefit from product test accuracy, reliable test solution, test cost saving and production cycle time to meet customer requirement.

2. METHODOLOGY

2.1 Overview

There are two most common methodologies used to evaluate ADC test performance which are Built-in-Self-Test (BIST) method and Histogram Method. From previous research (Gines et al., 2009), Adaptive BIST performs a blind and accurate estimation of the Integral Non-Linearity (INL) of the ADC under test without affecting to the normal converter operation, using any test stimuli or replicated hardware. Researcher (Gines et al., 2009), claims that adaptive BIST method avoids the on-chip generation of accurate test stimulus as no predefined input distribution is required. Furthermore, the analog signal path and ADC topology remains unmodified as there is not any additional input stimulus.

However, it requires additional digital logic and bank of registers to store the INL value. Thus, SOC need to reserve additional area for those registers and digital logic. In contrast with BIST method, histogram method does not require any overhead area for additional digital logic and registers.

![Fig. 3. Adaptive BIST method vs. Histogram method](Gines et al., 2009)
Furthermore, histogram test technique is more suitable for high volume testing because it is faster. Fig. 3 shows the INL comparison between Histogram and adaptive BIST method. From this result, INL for both methodologies are not differing much. INL for Histogram method slightly better at lower output code but for code higher than 6000 shows adaptive BIST and Histogram INL are about the same.

For Histogram method, previous researcher (Okawara, 2009) had derived Ramp and Sinusoidal Histogram algorithm to be used for ADC production testing. However, this algorithm has not yet been tested. There was no actual ADC test result from previous researcher. This work proposed test method flow and coding for ADC production testing using Histogram based methodologies. First methodology is histogram method using ramp as an input signal. Second methodology is histogram method using sine wave input signal. Fig. 4 shows the main flow that will be used in this research.

This research is started with ADC test program development for both methodologies. On these two methodologies, ADC parametric data will be compared with test specification inside Table 1. This test specification is not a global standard but it is recommended by the ADC designer. The actual specification could be revised once the ADC test achieve a good yield or low Part per Million (PPM) defect in actual production test run without affecting device reliability.

Typically, comparison on these two methodologies will be made based on statistical data. Based on the statistical analysis result, conclusion will be drawn.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Min</th>
<th>Max</th>
<th>Remarks</th>
</tr>
</thead>
<tbody>
<tr>
<td>DNL</td>
<td>-1 LSB</td>
<td>1 LSB</td>
<td>1 LSB = -2mV</td>
</tr>
<tr>
<td>INL</td>
<td>-3 LSB</td>
<td>3 LSB</td>
<td></td>
</tr>
<tr>
<td>Offset Error</td>
<td>-2 mV</td>
<td>2 mV</td>
<td></td>
</tr>
<tr>
<td>Gain Error</td>
<td>-6 mV</td>
<td>6 mV</td>
<td></td>
</tr>
</tbody>
</table>

Since this research objective is to get accurate and lower test cost for ADC, comparison is not only looking into the accuracy but it also look into the test time. The term optimize means looking for both aspect, accurate testing but with lower test cost possible. In evaluating ADC circuit in SOC, there are two elements that need to be considered which are static and dynamic. For high resolution ADC such as 16-bits above, the accuracy is definitely increased but the problem to take is more related to dynamic performance.

Using ATE as test equipment, RF subsystem is needed in investigating the dynamic performance. RF subsystem is very costly and it is not available in ATE that is being used for this research. For that reason, this research is only focusing on static performance measurement as an ADC evaluation. With static ADC parameters study, it is sufficient to evaluate 10-bits resolution ADC in high volume testing.

![Fig. 4 Research flow](image)

2.2 Histogram Test Procedure

Linearity is the most significant specification of ADC. There are several methods available to test linearity of ADC. Histogram method is the most common methodologies used in ADC linearity testing (IEEE, 2001). Histogram test technique sometimes is called as a code density test because each code has different number occurrences. Occurrences or number of hits per code is reflecting the density of code inside histogram plot. Ramp histogram and sinusoidal histogram test have been used for a long time.

However, linearity calculation equations for ramp and sinusoidal histogram are not well organized. In this research, histogram methods used based on the proposed technique by Hideo Okawara (2009). It is focusing on a terminal based (end-point) transfer function. Mathematical equations are introduced with using cumulative distribution function for Sinusoidal histogram. The method that is using this equation is free from overload level and offset of test signal sine wave so that test procedure is easier and faster in both hardware and software.

Tester configuration for linearity test using Verigy 93000 is as shown in Fig. 5. Histogram result is obtained using Test Method API to sort the elements of the specified array into the bins.
A procedure to generate linearity test for ADC is described as below:

1. Set DUT to the appropriate state.

2. Provide an analog input signal to the DUT. Input range has to be set -10% to -15% and +10 to +15% overload of full scale input range in order to make the DUT generate all available codes from 0 to 1023.

3. Capture raw output digital signal. In this particular test, 10 bits parallel data is captured using 10-bit vector variables. The output drivers can be configured to interface with full scale range of logic families.

4. Sort out the output code to create a histogram. Then, INL and DNL are calculated. The absolute maximum INL and DNL is the final result of DNL and INL respectively.

5. In order to make the DUT generate all available codes, the input stimulus must slightly overload to the input range. This is the most important criteria in histogram method. Input stimulus should swing from approximately -10% to 110% of the input range. Captured codes are sorted out creating a histogram as shown in Figure 6. Code 0 and code maximum are neglected due to invalid number of occurrence. Each bin count $H[i]$ is summed up from code 1 through $2^n-2$. Then the summation of $H[i]$ ($i=1...2^n-2$) is divided by $2^n-2$, and the average bin count $H_m$ is derived. Difference between each bin count $H[i]$ and $H_m$ is corresponding to differential non linearity (DNL). Cumulative value of DNL represents integral non linearity (INL). Histogram result is obtained using Test Method API to sort the elements of the specified array into the bins.

Apart from linearity test, Calculation of Gain and Offset Error as illustrated in Fig. 7 are the important criteria to evaluate ADC performance. Gain and Offset Error are calculated using Test Method API from the histogram analysis using (1) and (2). From Fig. 7, Gain Error is an error occurs near to the Full-Scale voltage whereas Offset Error is an error occurs near zero-scale voltage. There are only few MSB code density is being used for Gain Error calculation using histogram analysis. This research is using code density from 1.9V to 2.1V input voltage swing for Gain Error calculation. Code density for Offset Error calculation is only for -0.1V to 0.1V input voltage swing.

$$Gain Error = \frac{V_2 N_2 + V_3 N_1}{N_2 + N_3}$$

$$Offset Error = \frac{V_3 N_4 + V_0 N_1}{N_4 + N_1}$$

Where,
- $V_3$ = Full-Scale voltage
- $V_2$ = Voltage near Full-Scale voltage
- $V_1$ = Voltage near Zero-Scale Voltage
- $V_0$ = Zero-Scale voltage
- $N_3$ = Number of occurrences for Full-Scale voltage code
- $N_2$ = Summation number of occurrences for voltage near Full-Scale voltage code
- $N_1$ = Summation number of occurrences for voltage near Zero-Scale voltage code
- $N_0$ = Number of occurrences for Zero-Scale voltage code

2.3 Test Time Measurement

In ADC production testing, it is essential to develop test that has high accuracy with minimum test time. Theoretically
large sample size is good for ADC conversion accuracy. The drawback from the large sample size is the test time. More sample size will acquire more test time and this will impact the test cost (Gray, 2006).

3. RESULTS AND DISCUSSIONS

3.1 A Ramp and Sinusoidal Histogram Method Comparison

ADC linearity is the most important specification of ADC. In this research, there are two type of input that determines type of histogram method. Ramp method is a linear type of voltage supply increasing from the value of 0V until it reaches the full-scale voltage range. Sinusoidal histogram method is based on sine wave analog input supply. The algorithm to calculate ramp linearity is based on linear transfer function whereas sinusoidal linearity is based on probability density function (PDF). Ramp histogram pattern is different from sinusoidal histogram. Since sinusoidal histogram based on PDF, it appears a bath tub shape of histogram. The specification for DNL is +/-1LSB and specification for INL is +/-3LSB. The ideal case for non-error ADC conversion is 0LSB for both DNL and INL.

Figure 8 shows min DNL for both Ramp and Sinusoidal histogram methodology. From the results, linear trend line for min DNL were plotted and the trend indicate that min DNL for Sinusoidal histogram method exhibits lower than min DNL for Ramp histogram method. Therefore, Sinusoidal histogram method is better than Ramp histogram based on min DNL measurements.

Figure 9 shows max DNL for both Ramp and Sinusoidal histogram methodology. From the results, linear trend line for max DNL were plotted and the trend indicate that max DNL for Ramp histogram method is slightly lower than max DNL for Sinusoidal histogram method. Therefore, Ramp histogram method is better than Sinusoidal histogram based on max DNL measurements.

Figure 10 illustrate min INL for both Ramp and Sinusoidal histogram methodology. From the results, linear trend line for min INL were plot and the trend indicate that min INL for Ramp histogram method is lower than min INL for Sinusoidal histogram method. Therefore, Ramp histogram method is better than Sinusoidal histogram based on max DNL measurements.

Figure 11 illustrate max INL for both Ramp and Sinusoidal histogram methodology. From the results, linear trend line for max INL were plotted and the trend indicate that max INL for Sinusoidal histogram method is lower than max INL for Ramp histogram method. Therefore, Sinusoidal histogram method is better than Ramp histogram based on max DNL measurements.

In summary, both methods are accurate in terms of algorithm and calculation because it could be able to catch...
reject part. In production testing, test program should be able to segregate good and bad parts.

3.1 Test Time Measurement Result

In this research, ADC device is tested using dual site DUT board and hence parallel testing is introduced to reduce test cost. In high volume testing, both test cost and test accuracy is important to gain profit on device manufacturing. Table 2 shows the test time measurement result on single site and multi-site. It is clearly shows that test time per device for multi-site testing is greatly reduced. Multi site efficiency (MSE) is 63.72%. This number indicates that multi-site testing is 63.72% more efficient in term of testing time. ADC parallel testing should benefit from multi-site testing as the test accuracy is still preserve while the test cost is reduced.

Table 2. Test Time Measurement Result

<table>
<thead>
<tr>
<th>Measure name</th>
<th>Test time per flow (ms)</th>
<th>Test time per device (ms)</th>
<th>MSE (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Single Site</td>
<td>2347.951</td>
<td>2347.951</td>
<td></td>
</tr>
<tr>
<td>Multi-Site</td>
<td>3075.312</td>
<td>1537.657</td>
<td>63.72</td>
</tr>
</tbody>
</table>

4. CONCLUSIONS

The first objective of this research is to develop test solution for 28nm ADC with 10-bit resolution using ATE. This objective is the main contribution in this research. In first objective, ADC test flow and test method code has been developed to be used with ATE high volume testing. The test code has been developed based on optimized setting for internal reference voltage, sample size and sampling frequency. This research is using coherent sampling and the result clearly shows that ADC parameters were able to be measured using ADC test program. Second objective in this research is to evaluate ADC test performance with different input stimulus (Ramp and Sinusoidal). Based on the result on, Sinusoidal histogram has better measurement result on min DNL and max INL. Ramp histogram shows better result on max DNL and min INL. It was found that type of histogram methodology and the type of ADC parameters has no identical correlation. This means both histogram method algorithms and calculations used in this research are accurate. Both methods are suitable to be used as ADC production test methodology. Therefore, second objective was achieved. It is known that applying histogram methodology will acquire most testing time due to large sample size. However, with multi-site testing, ADC testing time can be reduced with MSE 63.72%. Hence, third objective on performing ADC parallel testing and test time reduction with multi-site testing was successfully achieved.

REFERENCES


